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# HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

## HITACHI

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### Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208  $5 \times 8$  dot character fonts and 32  $5 \times 10$  dot character fonts for a total of 240 different character fonts.

The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

### Features

- $5 \times 8$  and  $5 \times 10$  dot matrix possible
- Low power operation support:
  - 2.7 to 5.5V
- Wide range of liquid crystal display driver power
  - 3.0 to 11V
- Liquid crystal drive waveform
  - A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  - 2 MHz (when  $V_{cc} = 5V$ )
- 4-bit or 8-bit MPU interface enabled
- $80 \times 8$ -bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  - 208 character fonts ( $5 \times 8$  dot)
  - 32 character fonts ( $5 \times 10$  dot)

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## HD44780U

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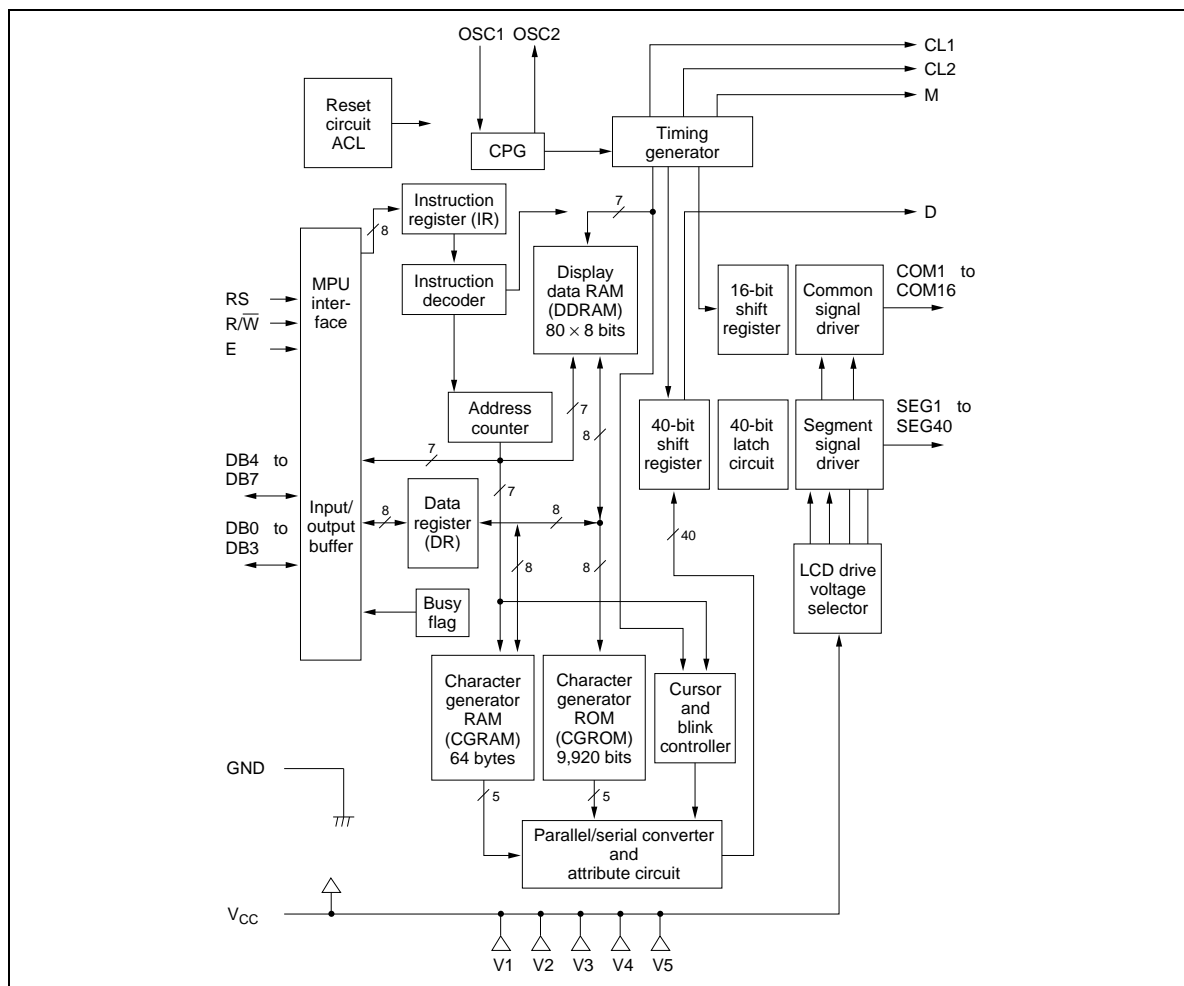
- 64 × 8-bit character generator RAM
  - 8 character fonts (5 × 8 dot)
  - 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of 5 × 8 dots with cursor
  - 1/11 for one line of 5 × 10 dots with cursor
  - 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

### Ordering Information

Type No.	Package	CGROM
HD44780UA00FS	FP-80B	Japanese standard font
HCD44780UA00	Chip	
HD44780UA00TF	TFP-80F	
HD44780UA02FS	FP-80B	European standard font
HCD44780UA02	Chip	
HD44780UA02TF	TFP-80F	
HD44780UBxxFS	FP-80B	Custom font
HCD44780UBxx	Chip	
HD44780UBxxTF	TFP-80F	

Note: xx: ROM code No.

# HD44780U Block Diagram

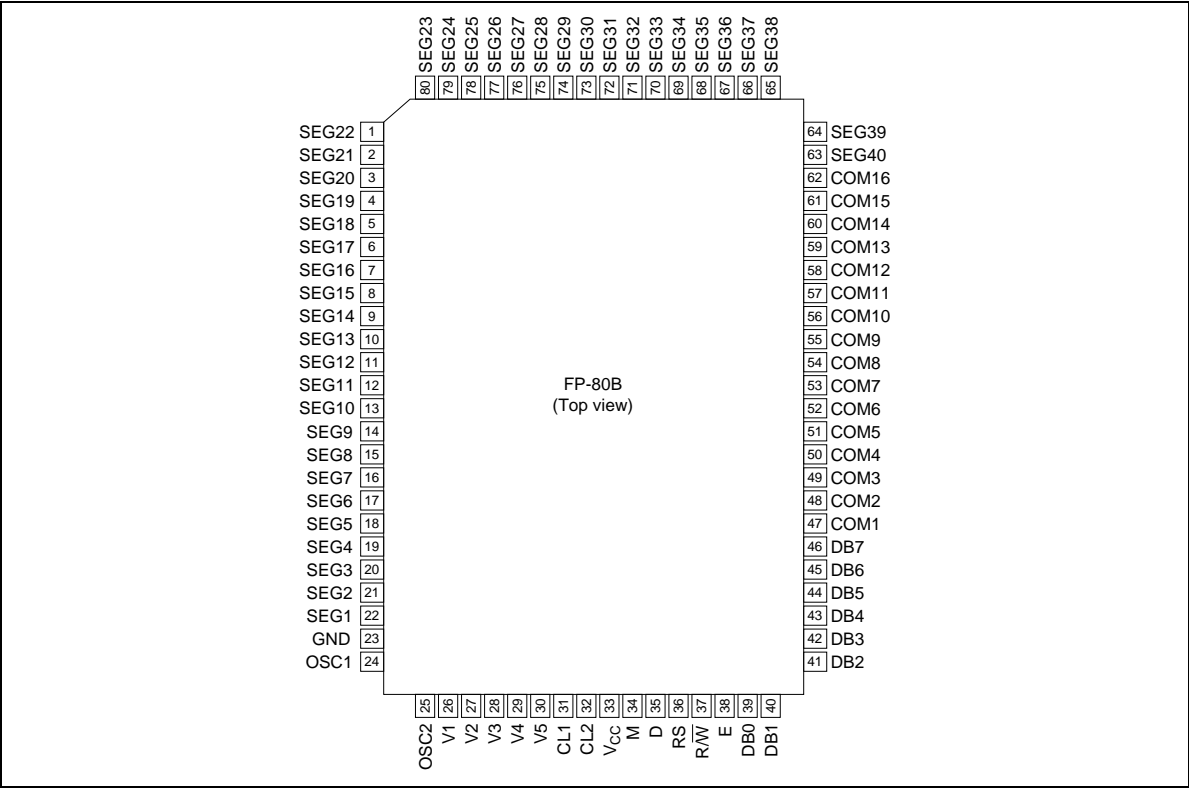


## HD44780U

### LCD-II Family Comparison

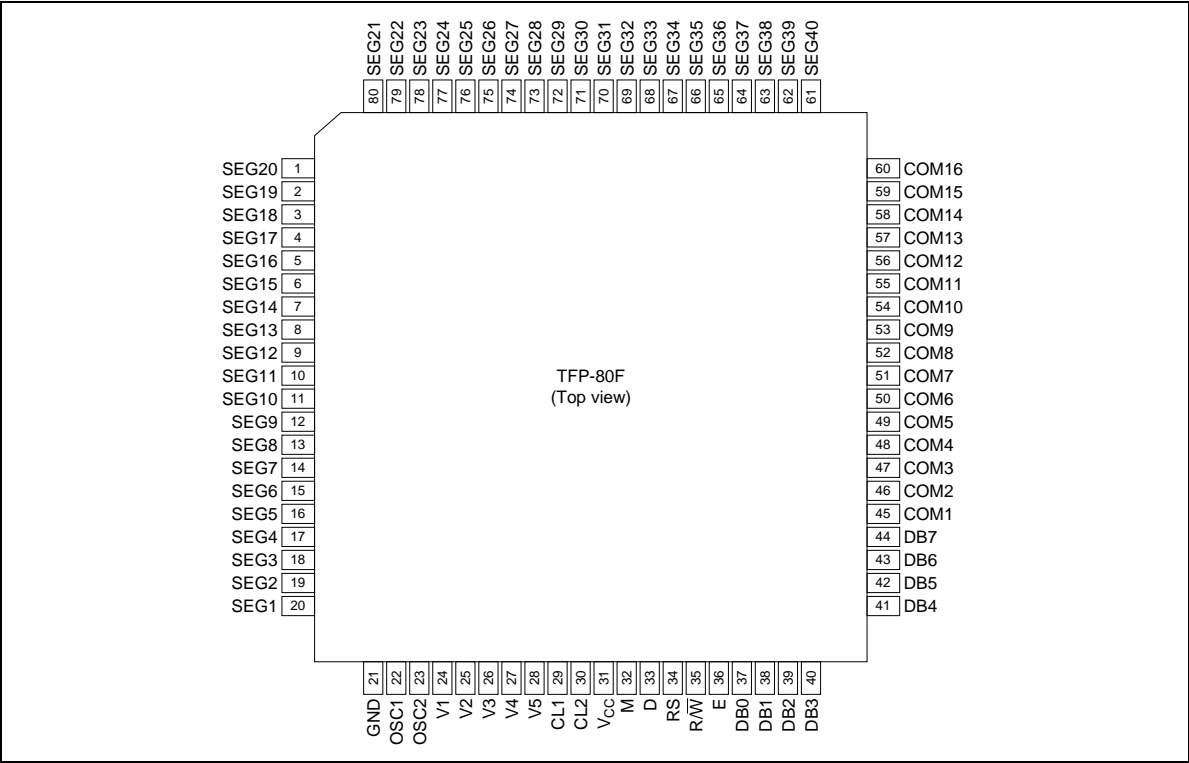
Item		HD44780S	HD44780U
Power supply voltage		5 V $\pm 10\%$	2.7 to 5.5 V
Liquid crystal drive voltage VLCD	1/4 bias	3.0 to 11.0V	3.0 to 11.0V
	1/5 bias	4.6 to 11.0V	3.0 to 11.0V
Maximum display digits per chip		16 digits (8 digits $\times$ 2 lines)	16 digits (8 digits $\times$ 2 lines)
Display duty cycle		1/8, 1/11, and 1/16	1/8, 1/11, and 1/16
CGROM		7,200 bits (160 character fonts for 5 $\times$ 7 dot and 32 character fonts for 5 $\times$ 10 dot)	9,920 bits (208 character fonts for 5 $\times$ 8 dot and 32 character fonts for 5 $\times$ 10 dot)
CGRAM		64 bytes	64 bytes
DDRAM		80 bytes	80 bytes
Segment signals		40	40
Common signals		16	16
Liquid crystal drive waveform		A	A
Oscillator	Clock source	External resistor, external ceramic filter, or external clock	External resistor or external clock
	R <sub>i</sub> oscillation frequency (frame frequency)	270 kHz $\pm 30\%$ (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)	270 kHz $\pm 30\%$ (59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle)
	R <sub>i</sub> resistance	91 k $\Omega$ $\pm 2\%$	91 k $\Omega$ $\pm 2\%$ (when V <sub>cc</sub> = 5V) 75 k $\Omega$ $\pm 2\%$ (when V <sub>cc</sub> = 3V)
Instructions		Fully compatible within the HD44780S	
CPU bus timing		1 MHz	1 MHz (when V <sub>cc</sub> = 3V) 2 MHz (when V <sub>cc</sub> = 5V)
Package		FP-80 FP-80A	FP-80B TFP-80F

HD44780U Pin Arrangement (FP-80B)

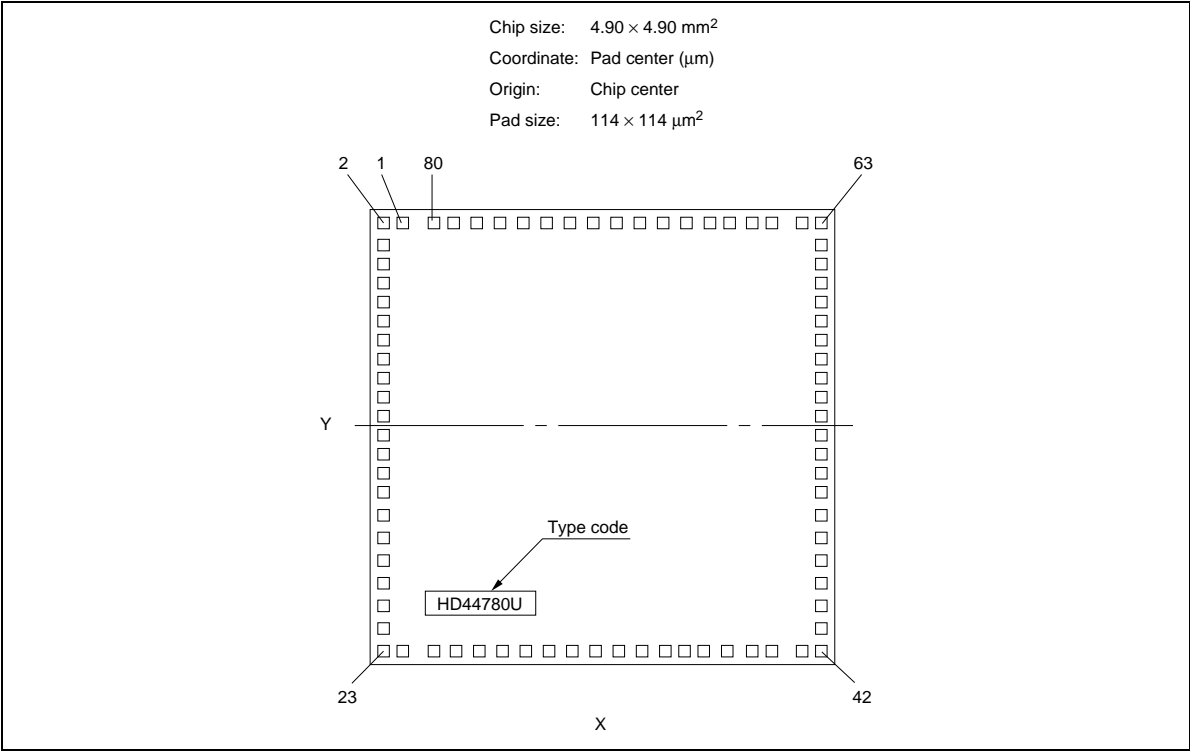


HD44780U

HD44780U Pin Arrangement (TFP-80F)



HD44780U Pad Arrangement



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**HD44780U**

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**HCD44780U Pad Location Coordinates**

Pad No.	Function	Coordinate	
		X (um)	Y (um)
1	SEG22	-2100	2313
2	SEG21	-2280	2313
3	SEG20	-2313	2089
4	SEG19	-2313	1833
5	SEG18	-2313	1617
6	SEG17	-2313	1401
7	SEG16	-2313	1186
8	SEG15	-2313	970
9	SEG14	-2313	755
10	SEG13	-2313	539
11	SEG12	-2313	323
12	SEG11	-2313	108
13	SEG10	-2313	-108
14	SEG9	-2313	-323
15	SEG8	-2313	-539
16	SEG7	-2313	-755
17	SEG6	-2313	-970
18	SEG5	-2313	-1186
19	SEG4	-2313	-1401
20	SEG3	-2313	-1617
21	SEG2	-2313	-1833
22	SEG1	-2313	-2073
23	GND	-2280	-2290
24	OSC1	-2080	-2290
25	OSC2	-1749	-2290
26	V1	-1550	-2290
27	V2	-1268	-2290
28	V3	-941	-2290
29	V4	-623	-2290
30	V5	-304	-2290
31	CL1	-48	-2290
32	CL2	142	-2290
33	V <sub>cc</sub>	309	-2290
34	M	475	-2290
35	D	665	-2290
36	RS	832	-2290
37	R/W	1022	-2290
38	E	1204	-2290
39	DB0	1454	-2290
40	DB1	1684	-2290

Pad No.	Function	Coordinate	
		X (um)	Y (um)
41	DB2	2070	-2290
42	DB3	2260	-2290
43	DB4	2290	-2099
44	DB5	2290	-1883
45	DB6	2290	-1667
46	DB7	2290	-1452
47	COM1	2313	-1186
48	COM2	2313	-970
49	COM3	2313	-755
50	COM4	2313	-539
51	COM5	2313	-323
52	COM6	2313	-108
53	COM7	2313	108
54	COM8	2313	323
55	COM9	2313	539
56	COM10	2313	755
57	COM11	2313	970
58	COM12	2313	1186
59	COM13	2313	1401
60	COM14	2313	1617
61	COM15	2313	1833
62	COM16	2313	2095
63	SEG40	2296	2313
64	SEG39	2100	2313
65	SEG38	1617	2313
66	SEG37	1401	2313
67	SEG36	1186	2313
68	SEG35	970	2313
69	SEG34	755	2313
70	SEG33	539	2313
71	SEG32	323	2313
72	SEG31	108	2313
73	SEG30	-108	2313
74	SEG29	-323	2313
75	SEG28	-539	2313
76	SEG27	-755	2313
77	SEG26	-970	2313
78	SEG25	-1186	2313
79	SEG24	-1401	2313
80	SEG23	-1617	2313



**Pin Functions**

Signal	No. of Lines	I/O	Device Interfaced with	Function
RS	1	I	MPU	Selects registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/W	1	I	MPU	Selects read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. These pins are not used during 4-bit operation.
CL1	1	O	Extension driver	Clock to latch serial data D sent to the extension driver
CL2	1	O	Extension driver	Clock to shift serial data D
M	1	O	Extension driver	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	Extension driver	Character pattern data corresponding to each segment signal
COM1 to COM16	16	O	LCD	Common signals that are not used are changed to non-selection waveforms. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor.
SEG1 to SEG40	40	O	LCD	Segment signals
V1 to V5	5	—	Power supply	Power supply for LCD drive $V_{cc} - V5 = 11\text{ V (max)}$
$V_{cc}$ , GND	2	—	Power supply	$V_{cc}$ : 2.7V to 5.5V, GND: 0V
OSC1, OSC2	2	—	Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.

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## HD44780U

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### Function Description

#### Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DDRAM or CGRAM and temporarily stores data to be read from DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into DDRAM or CGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM or CGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM or CGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 1).

#### Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When  $RS = 0$  and  $R/\overline{W} = 1$  (Table 1), the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

#### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when  $RS = 0$  and  $R/\overline{W} = 1$  (Table 1).

**Table 1     Register Selection**

RS	R/ $\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	DR write as an internal operation (DR to DDRAM or CGRAM)
1	1	DR read as an internal operation (DDRAM or CGRAM to DR)

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is  $80 \times 8$  bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address ( $A_{DD}$ ) is set in the address counter (AC) as hexadecimal.

- 1-line display ( $N = 0$ ) (Figure 2)
  - When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See Figure 3.
  - When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

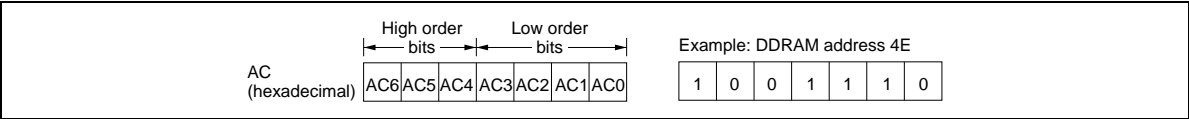


Figure 1 DDRAM Address

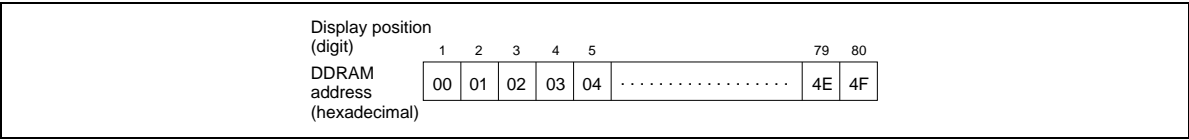


Figure 2 1-Line Display

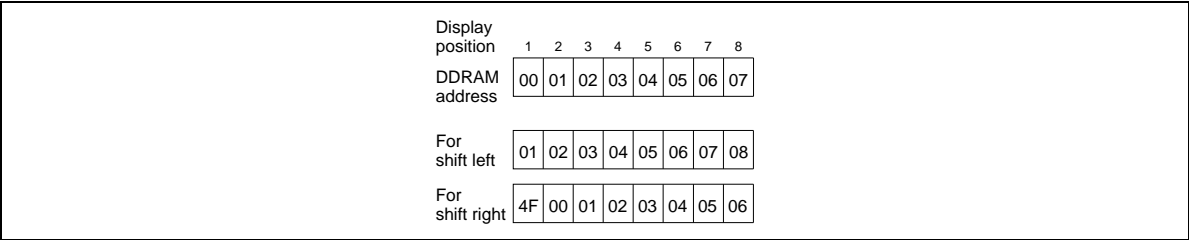


Figure 3 1-Line by 8-Character Display Example

- 2-line display (N = 1) (Figure 4)
  - Case 1: When the number of display characters is less than  $40 \times 2$  lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters  $\times$  2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

### Figure 4 2-Line Display

### Figure 5 2-Line by 8-Character Display Example

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

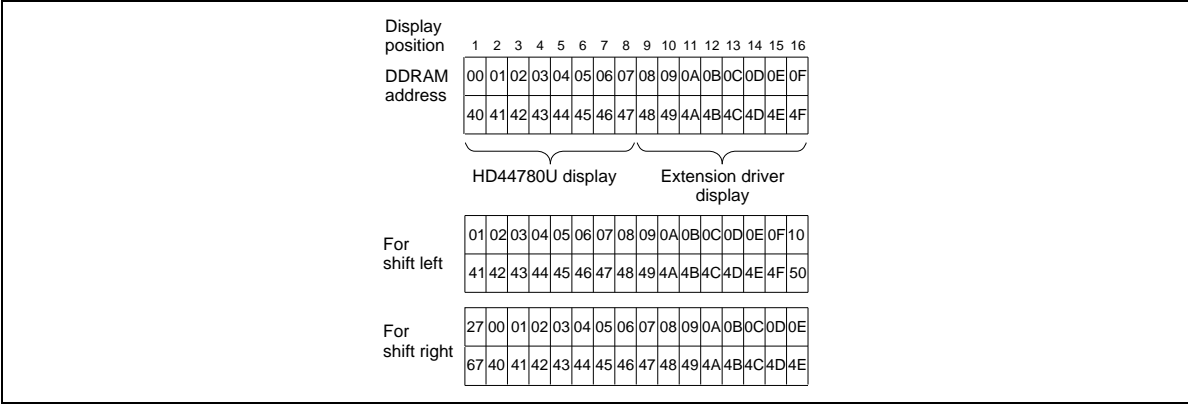


Figure 6 2-Line by 16-Character Display Example

**Character Generator ROM (CGROM)**

The character generator ROM generates  $5 \times 8$  dot or  $5 \times 10$  dot character patterns from 8-bit character codes (Table 4). It can generate 208  $5 \times 8$  dot character patterns and 32  $5 \times 10$  dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

**Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For  $5 \times 8$  dots, eight character patterns can be written, and for  $5 \times 10$  dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

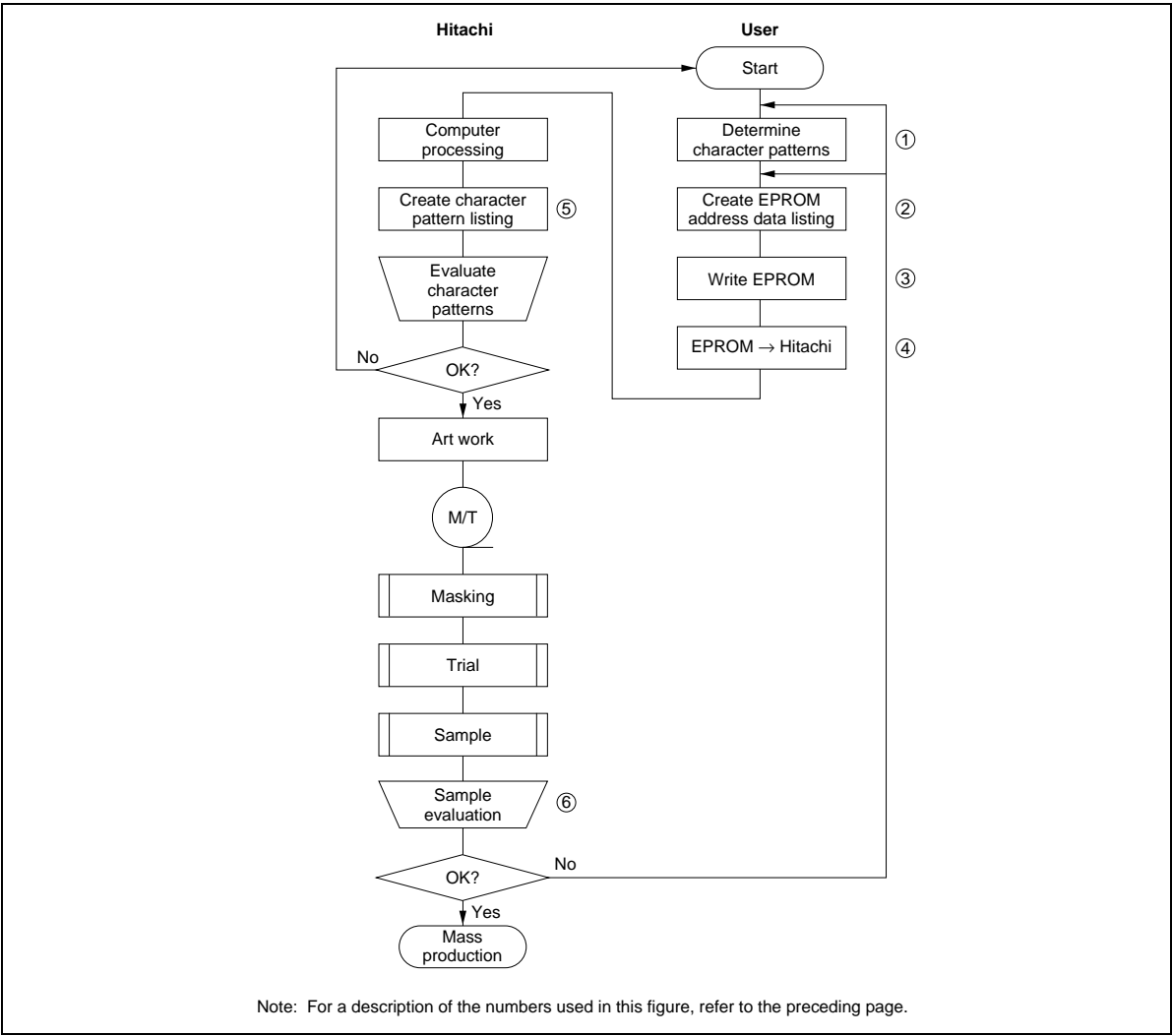
Areas that are not used for display can be used as general data RAM.

**Modifying Character Patterns**

- Character pattern development procedure

The following operations correspond to the numbers listed in Figure 7:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



**Figure 7 Character Pattern Development Procedure**





— Handling unused character patterns

1. EPROM data outside the character pattern area: Always input 0s.
2. EPROM data in CGRAM area: Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)
3. EPROM data used when the user does not use any HD44780U character pattern: According to the user application, handled in one of the two ways listed as follows.
  - a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)
  - b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

**Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 Dots)**

EPROM Address												Data								
												LSB								
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0				
0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0				
												0	0	0	1	0	0	0	0	0
												0	0	1	0	0	1	1	0	1
												0	0	1	1	1	0	0	1	1
												0	1	0	0	1	0	0	0	1
												0	1	0	1	1	0	0	0	1
												0	1	1	0	0	1	1	1	1
												0	1	1	1	0	0	0	0	1
												1	0	0	0	0	0	0	0	1
												1	0	0	1	0	0	0	0	1
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												1	0	1	0	0				
												1	0	1	1	0	0	0	0	
												1	1	0	0	0	0	0	0	
												1	1	0	1	0	0	0	0	
												1	1	1	0	0	0	0	0	
												1	1	1	1	0	0	0	0	

Character code

Line position

Cursor position

- Notes:
1. EPROM addresses A11 to A3 correspond to a character code.
  2. EPROM addresses A3 to A0 specify a line position of the character pattern.
  3. EPROM data O4 to O0 correspond to character pattern data.
  4. EPROM data O5 to O7 must be specified as 0.
  5. A lit display position (black) corresponds to a 1.
  6. Line 11 and the following lines must be blanked with 0s for a 5 × 10 dot character fonts.

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**Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)**

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	a	P	`	P				-	9	3	o	p
xxxx0001	(2)		!	1	A	Q	a	9				2	7	4	ä	q
xxxx0010	(3)		"	2	B	R	b	r				「	イ	ツ	×	þ
xxxx0011	(4)		#	3	C	S	c	s				」	ウ	テ	ε	ω
xxxx0100	(5)		\$	4	D	T	d	t				、	エ	ト	†	μ
xxxx0101	(6)		%	5	E	U	e	u				・	オ	ナ	1	σ
xxxx0110	(7)		&	6	F	V	f	v				ヲ	カ	ニ	ヨ	ρ
xxxx0111	(8)		'	7	G	W	g	w				フ	キ	ヌ	ラ	π
xxxx1000	(1)		(	8	H	X	h	x				イ	ウ	ネ	リ	フ
xxxx1001	(2)		)	9	I	Y	i	y				6	7	ノ	ル	´
xxxx1010	(3)		*	:	J	Z	j	z				エ	コ	ハ	レ	j
xxxx1011	(4)		+	;	K	L	k	{				オ	サ	ヒ	ロ	×
xxxx1100	(5)		,	<	L	¥	1					†	シ	フ	ワ	φ
xxxx1101	(6)		-	=	M	I	m	}				ユ	ズ	ハ	ン	÷
xxxx1110	(7)		.	>	N	^	n	+				ヨ	セ	ホ	°	ñ
xxxx1111	(8)		/	?	0	_	o	+				ッ	リ	マ	°	■

Note: The user can specify any pattern for character-generator RAM.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)

Lower 4 Bits	Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		▶		0	Q	P	`	F	E	o		°	À	Ð	á	ÿ
xxxx0001	(2)		¶	!	1	A	Q	a	¶	A	J	i	±	Á	Ñ	á	ñ
xxxx0010	(3)		“	”	2	B	R	b	r	W	Γ	Q	²	Â	Ò	â	ò
xxxx0011	(4)		”	#	3	C	S	c	s	3	π	ℓ	³	Ã	Ó	ã	ó
xxxx0100	(5)		⌂	\$	4	D	T	d	t	M	Σ	×	℔	Ä	Ö	ä	ö
xxxx0101	(6)		₣	%	5	E	U	e	u	ñ	σ	¥	¥	Å	Ö	ä	ö
xxxx0110	(7)		•	&	6	F	V	f	v	J	¶	!	¶	Æ	Ö	æ	ö
xxxx0111	(8)		¶	'	7	G	W	w	¶	τ	§	•	¶	×	¶	÷	
xxxx1000	(1)		†	(	8	H	X	h	x	Y	¶	¶	o	É	¶	é	¶
xxxx1001	(2)		‡	)	9	I	Y	i	y	U	¶	¶	¹	Ê	Ù	ê	ù
xxxx1010	(3)		÷	*	:	J	Z	j	z	4	Q	¶	¶	Ê	Ù	ê	ù
xxxx1011	(4)		¶	+	:	K	I	k	{	W	¶	¶	¶	Ê	Ù	ê	ù
xxxx1100	(5)		≤	,	<	L	\	l	l	W	¶	¶	¶	Ë	Û	ë	û
xxxx1101	(6)		≥	-	=	M	I	m	}	b	¶	¶	¶	Ë	Û	ë	û
xxxx1110	(7)		▲	.	>	N	^	n	~	W	¶	¶	¶	Ë	Û	ë	û
xxxx1111	(8)		₣	/	?	O	_	o	o	3	¶	¶	¶	Ë	Û	ë	û

**Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)**

For 5 × 8 dot character patterns																									
Character Codes (DDRAM data)								CGRAM Address		Character Patterns (CGRAM data)															
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0				
High				Low				High		Low		High				Low									
0 0 0 0 * 0 0 0								0 0 0		0	0	0					*	*	*	1	1	1	1	0	Character pattern (1)
										0	0	1					1	0	0	0	1	Cursor position			
										0	1	0					1	0	0	0	1				
										0	1	1					1	1	1	1	0				
										1	0	0					1	0	1	0	0				
										1	0	1					1	0	0	1	0				
										1	1	0					1	0	0	0	1				
										1	1	1					*	*	*	0	0		0	0	
0 0 0 0 * 0 0 1								0 0 1		0	0	0					*	*	*	1	0	0	0	1	Character pattern (2)
										0	0	1					0	1	0	1	0	Cursor position			
										0	1	0					1	1	1	1	1				
										0	1	1					0	0	1	0	0				
										1	0	0					1	1	1	1	1				
										1	0	1					0	0	1	0	0				
										1	1	0					0	0	1	0	0				
										1	1	1					*	*	*	0	0		0	0	
0 0 0 0 * 1 1 1								1 1 1		0	0	0					*	*	*					Cursor position	
										0	0	1					*	*	*						
0 0 0 0 * 1 1 1								1 1 1		1	0	0													
										1	0	1													
										1	1	0													
										1	1	1													
										1	1	1					*	*	*						

- Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
- Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.
- If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- \* Indicates no effect.

**Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data) (cont)**

For 5 × 10 dot character patterns																													
Character Codes (DDRAM data)								CGRAM Address								Character Patterns (CGRAM data)													
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0								
High				Low				High				Low				High				Low									
0 0 0 0 * 0 0 *								0 0								0	0	0	0	*	*	*	0	0	0	0	Character pattern		
																0	0	0	1	0	0	0	0	0	0	0		0	
																0	0	1	0	0	0	1	1	1	0	1		1	
																0	1	0	0	0	1	1	0	1	0	0		1	
																0	1	1	0	0	1	1	0	1	0	0		1	
																0	1	1	1	0	0	0	0	1	1	1		1	
																1	0	0	0	1	0	0	0	1	0	0		0	
																1	0	0	1	0	0	0	0	1	0	0		0	
																1	0	1	0	0	0	0	0	0	0	0		0	0
1	0	1	1	0	0	0	0	0	0	0	0																		
1	1	0	0	0	0	0	0	0	0	0	0																		
1	1	0	1	0	0	0	0	0	0	0	0																		
1	1	1	0	0	0	0	0	0	0	0	0																		
																0	0	0	0	0	0	0	0	0	0				
																0	0	0	1	0	0	0	0	0	0		0	0	
																1	0	1	1	0	0	0	0	0	0		0	0	
																1	1	1	0	0	0	0	0	0	0		0	0	
																1	1	1	1	0	0	0	0	0	0		0	0	
0 0 0 0 * 1 1 *								1 1								1	0	0	1	*	*	*	*	*	*	*			
																1	0	1	0	0	1	0	0	0	0	0		0	
																1	0	1	0	0	1	0	0	0	0	0		0	
																1	1	0	0	1	0	0	0	0	0	0		0	
																1	1	1	0	0	1	0	0	0	0	0		0	
																1	0	0	1	*	*	*	*	*	*	*			
																1	0	1	0	0	1	0	0	0	0	0		0	
																1	1	0	0	1	0	0	0	0	0	0		0	
																1	1	1	0	0	1	0	0	0	0	0		0	
																1	1	1	1	0	0	0	0	0	0	0		0	

- Notes:
- Character code bits 1 and 2 correspond to CGRAM address bits 4 and 5 (2 bits: 4 types).
  - CGRAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.  
Maintain the 11th line data corresponding to the cursor display position at 0 as the cursor display.  
If the 11th line data is "1", "1" bits will light up the 11th line regardless of the cursor presence.  
Since lines 12 to 16 are not used for display, they can be used for general data RAM.
  - Character pattern row positions are the same as 5 × 8 dot character pattern positions.
  - CGRAM character patterns are selected when character code bits 4 to 7 are all 0.  
However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.
  - 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- \* Indicates no effect.

## Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

## Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

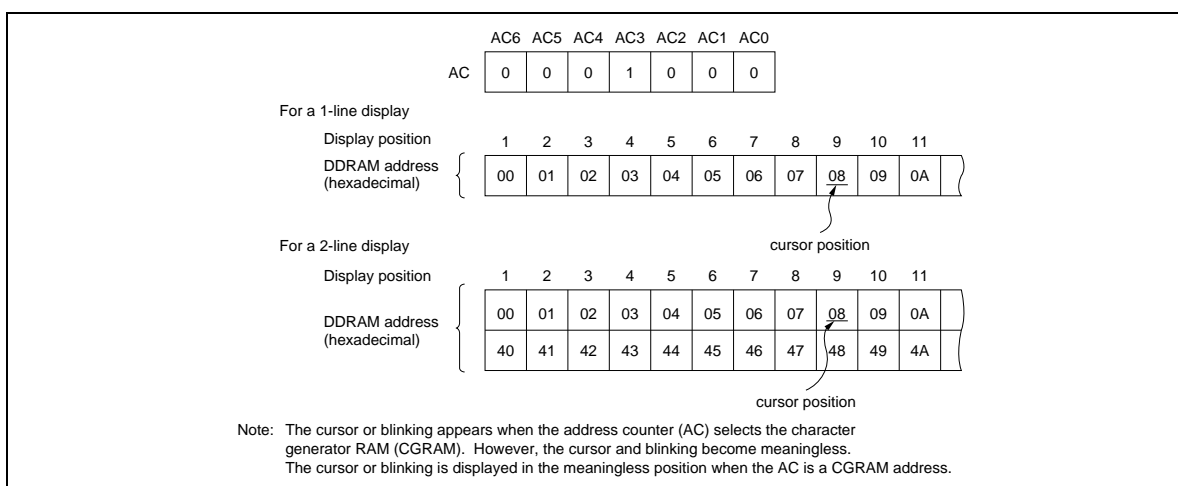
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display.

## Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example (Figure 8), when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.



**Figure 8 Cursor/Blink Display Example**

## Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).

The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

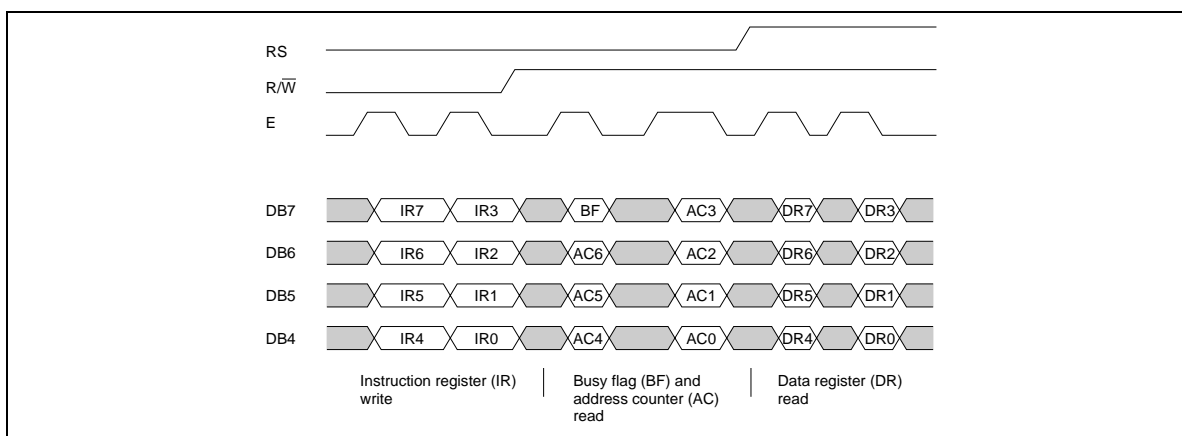


Figure 9 4-Bit Transfer Example

## **Reset Function**

### **Initializing by Internal Reset Circuit**

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after  $V_{CC}$  rises to 4.5 V.

1. Display clear
2. Function set:
  - DL = 1; 8-bit interface data
  - N = 0; 1-line display
  - F = 0;  $5 \times 8$  dot character font
3. Display on/off control:
  - D = 0; Display off
  - C = 0; Cursor off
  - B = 0; Blinking off
4. Entry mode set:
  - I/D = 1; Increment by 1
  - S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

## **Instructions**

### **Outline**

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/

write signal ( $R/\overline{W}$ ), and the data bus (DB0 to DB7), make up the HD44780U instructions (Table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions



Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state ( $BF = 0$ ) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 6 for the list of each instruction execution time.

**Table 6 Instructions**

Instruction	Code										Description	Execution Time (max) (when $f_{cp}$ or $f_{osc}$ is 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 $\mu$ s
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 $\mu$ s
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 $\mu$ s
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 $\mu$ s
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 $\mu$ s
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 $\mu$ s
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 $\mu$ s

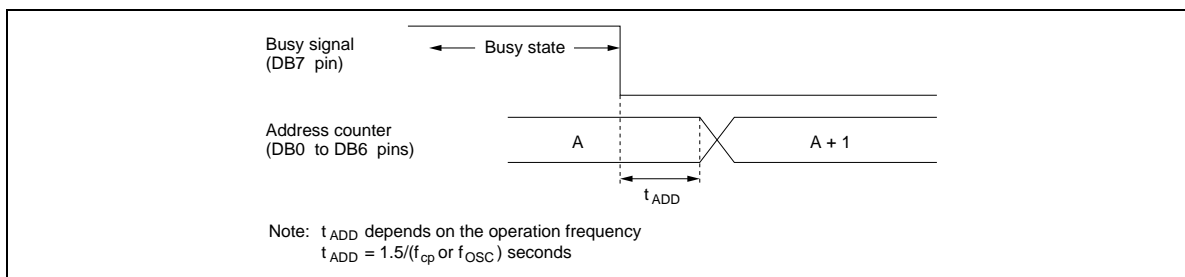
# HD44780U

**Table 6 Instructions (cont)**

Instruction	Code										Description	Execution Time (max) (when $f_{cp}$ or
	RS	R/ $\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		$f_{OSC}$ is 270 kHz)
Write data to CG or DDRAM	1	0	Write data								Writes data into DDRAM or CGRAM.	37 $\mu$ s $t_{ADD} = 4 \mu$ s*
Read data from CG or DDRAM	1	1	Read data								Reads data from DDRAM or CGRAM.	37 $\mu$ s $t_{ADD} = 4 \mu$ s*
	I/D = 1:	Increment								DDRAM: Display data RAM	Execution time changes when frequency changes Example: When $f_{cp}$ or $f_{OSC}$ is 250 kHz, $37 \mu$ s $\times \frac{270}{250} = 40 \mu$ s	
	I/D = 0:	Decrement								CGRAM: Character generator RAM		
	S = 1:	Accompanies display shift								RAM		
	S/C = 1:	Display shift								ACG: CGRAM address		
	S/C = 0:	Cursor move								ADD: DDRAM address		
	R/L = 1:	Shift to the right								(corresponds to cursor address)		
	R/L = 0:	Shift to the left										
	DL = 1:	8 bits, DL = 0: 4 bits								AC: Address counter used for both DD and CGRAM addresses		
	N = 1:	2 lines, N = 0: 1 line										
	F = 1:	5 $\times$ 10 dots, F = 0: 5 $\times$ 8 dots										
	BF = 1:	Internally operating										
	BF = 0:	Instructions acceptable										

Note: — indicates no effect.

- \* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10,  $t_{ADD}$  is the time elapsed after the busy flag turns off until the address counter is updated.



**Figure 10 Address Counter Update**

## Instruction Description

### Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

### Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

### Entry Mode Set

**I/D:** Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.

**S:** Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

### Display On/Off Control

**D:** The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

**C:** The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for  $5 \times 8$  dot character font selection and in the 11th line for the  $5 \times 10$  dot character font selection (Figure 13).

**B:** The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when  $f_{cp}$  or  $f_{osc}$  is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to  $f_{osc}$  or the reciprocal of  $f_{cp}$ . For example, when  $f_{cp}$  is 270 kHz,  $409.6 \times 250/270 = 379.2$  ms.)

### **Cursor or Display Shift**

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

### **Function Set**

**DL:** Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0. When 4-bit length is selected, data must be sent or received twice.

**N:** Sets the number of display lines.

**F:** Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

### **Set CGRAM Address**

Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

[illegible]

**Figure 11**

Cursor or display shift	Code	RS	R/ $\bar{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note: * Don't care.
		0	0	0	0	0	1	S/C	R/L	*	*	
Function set	Code	RS	R/ $\bar{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
		0	0	0	0	0	DL	N	F	*	*	
Set CGRAM address	Code	RS	R/ $\bar{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
		0	0	0	0	A	A	A	A	A	A	
						Higher order bit			Lower order bit			

**Figure 12**

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## HD44780U

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### Set DDRAM Address

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DDRAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

### Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DDRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CGRAM address and set DDRAM address.

**Table 7      Shift Function**

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

**Table 8      Function Set**

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5 × 8 dots	1/8	
0	1	1	5 × 10 dots	1/11	
1	*	2	5 × 8 dots	1/16	Cannot display two lines for 5 × 10 dot character font

Note: \* Indicates don't care.

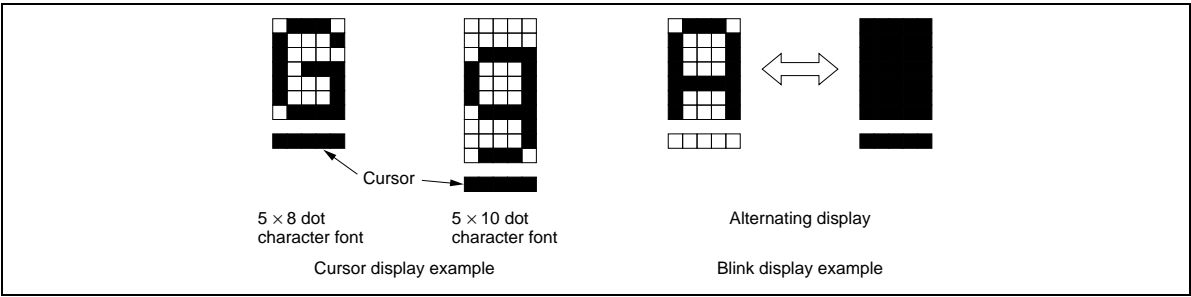


Figure 13 Cursor and Blinking

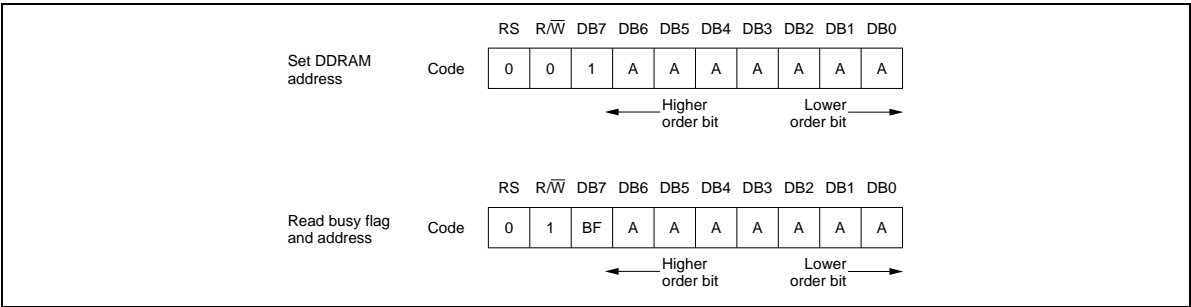


Figure 14

### Write Data to CG or DDRAM

Write data to CG or DDRAM writes 8-bit binary data DDDDDDDD to CG or DDRAM.

To write into CG or DDRAM is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

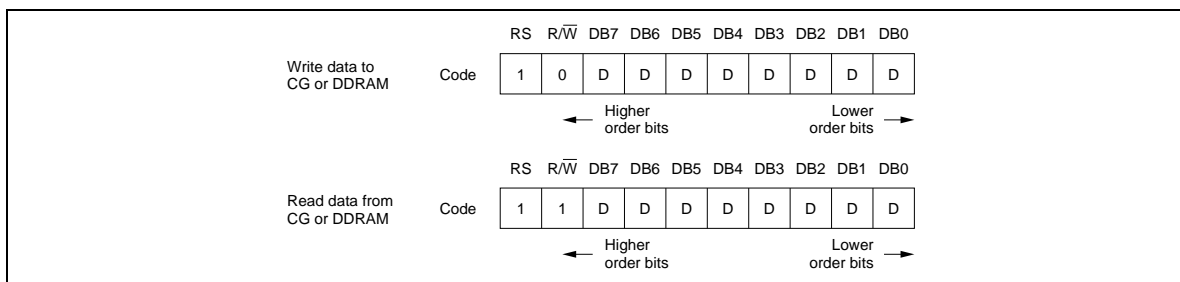
### Read Data from CG or DDRAM

Read data from CG or DDRAM reads 8-bit binary data DDDDDDDD from CG or DDRAM.

The previous designation determines whether CG or DDRAM is to be read. Before entering this read instruction, either CGRAM or DDRAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DDRAM). The operation of the cursor shift instruction is the same as the set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CGRAM or DDRAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DDRAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.



**Figure 15**



Interfacing the HD44780U

Interface to MPUs

- Interfacing to an 8-bit MPU  
See Figure 17 for an example of using a I/O port (for a single-chip microcomputer) as an interface device.  
In this example, P30 to P37 are connected to the data bus DB0 to DB7, and P75 to P77 are connected to E, R/W, and RS, respectively.

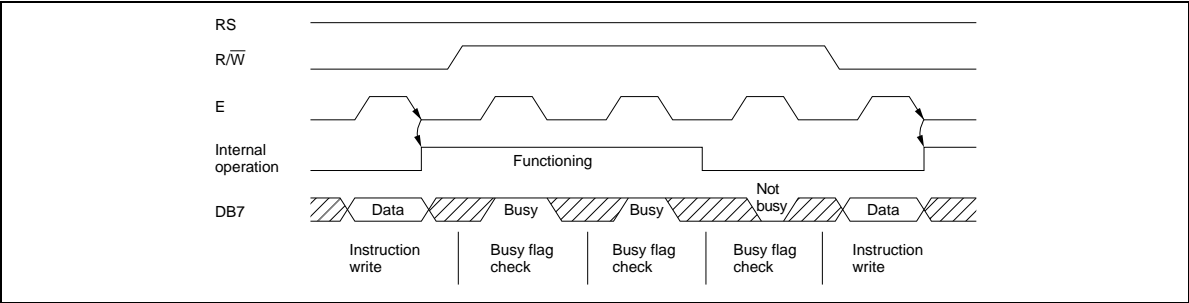


Figure 16 Example of Busy Flag Check Timing Sequence

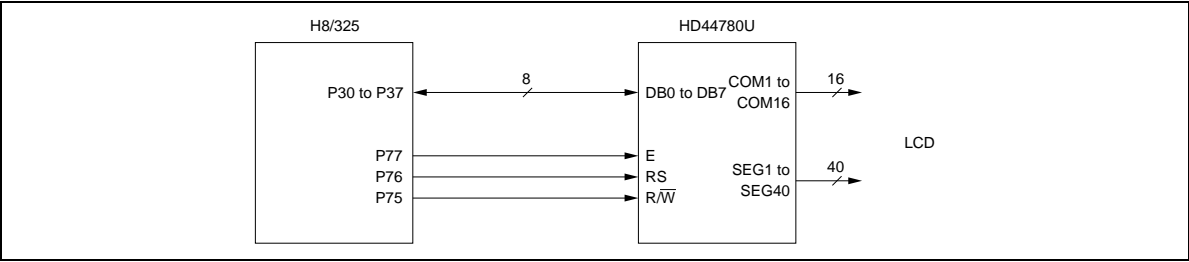


Figure 17 H8/325 Interface (Single-Chip Mode)

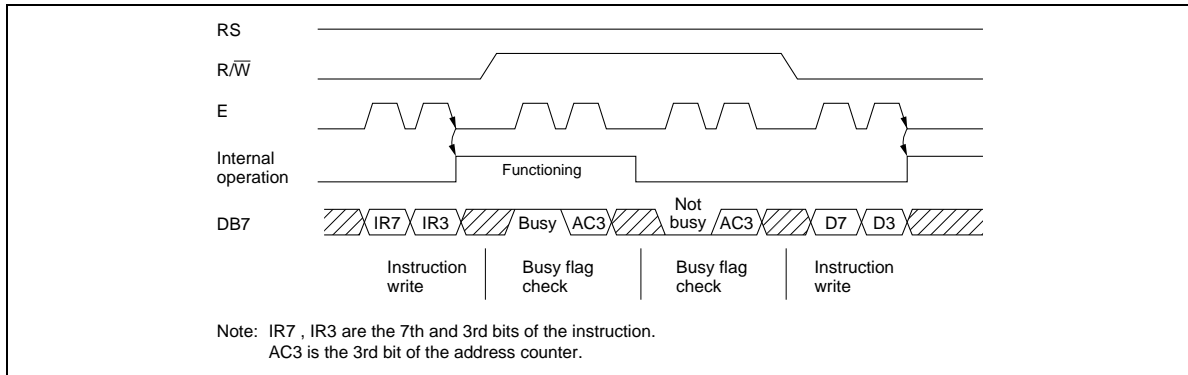
## HD44780U

- Interfacing to a 4-bit MPU

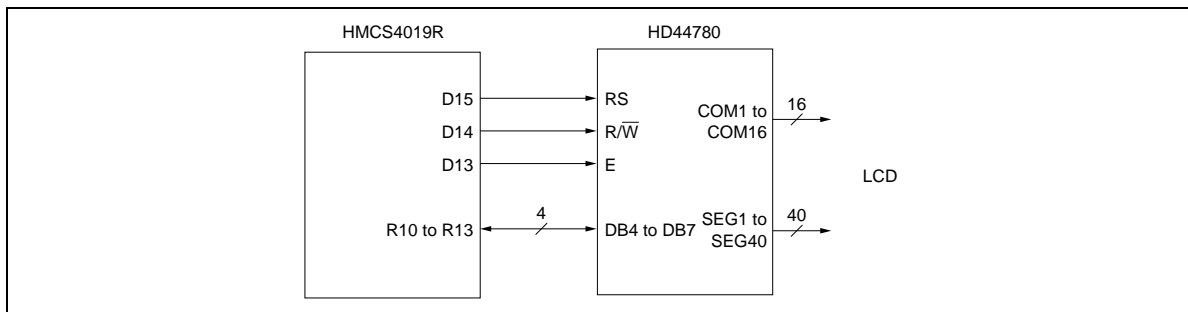
The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See Figure 18.)

See Figure 19 for an interface example to the HMCS4019R.

Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.



**Figure 18 Example of 4-Bit Data Transfer Timing Sequence**



**Figure 19 Example of Interface to HMCS4019R**

### Interface to Liquid Crystal Display

**Character Font and Number of Lines:** The HD44780U can perform two types of displays,  $5 \times 8$  dot and  $5 \times 10$  dot character fonts, each with a cursor.

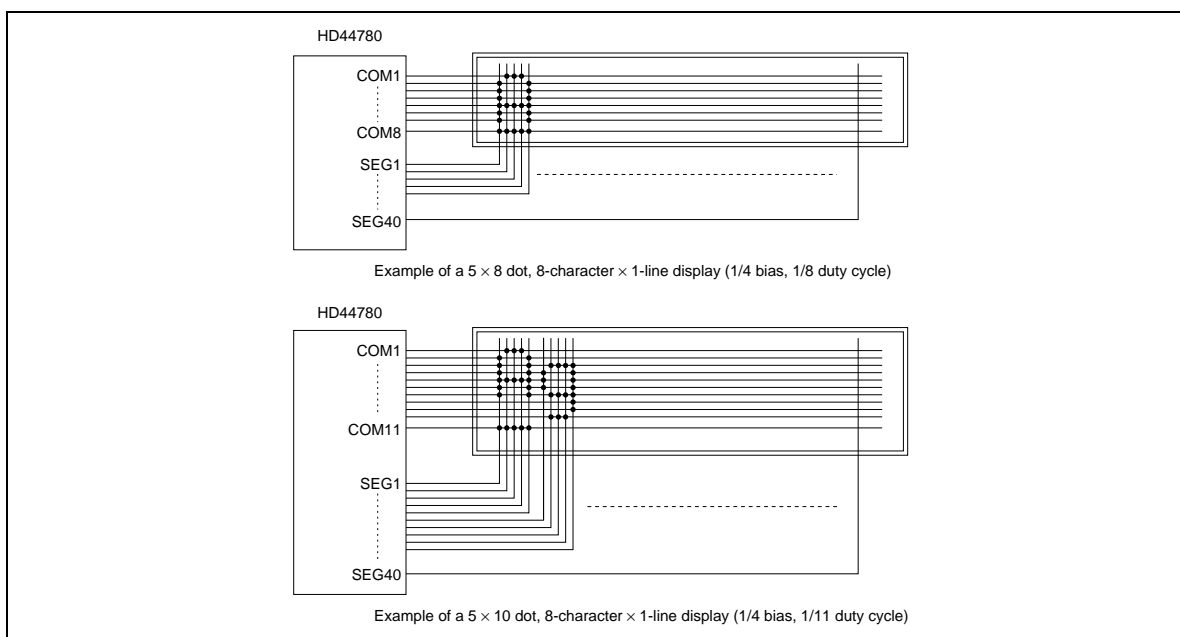
Up to two lines are displayed for  $5 \times 8$  dots and one line for  $5 \times 10$  dots. Therefore, a total of three types of common signals are available (Table 9).

The number of lines and font types can be selected by the program. (See Table 6, Instructions.)

**Connection to HD44780 and Liquid Crystal Display:** See Figure 20 for the connection examples.

**Table 9 Common Signals**

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	$5 \times 8$ dots + cursor	8	1/8
1	$5 \times 10$ dots + cursor	11	1/11
2	$5 \times 8$ dots + cursor	16	1/16

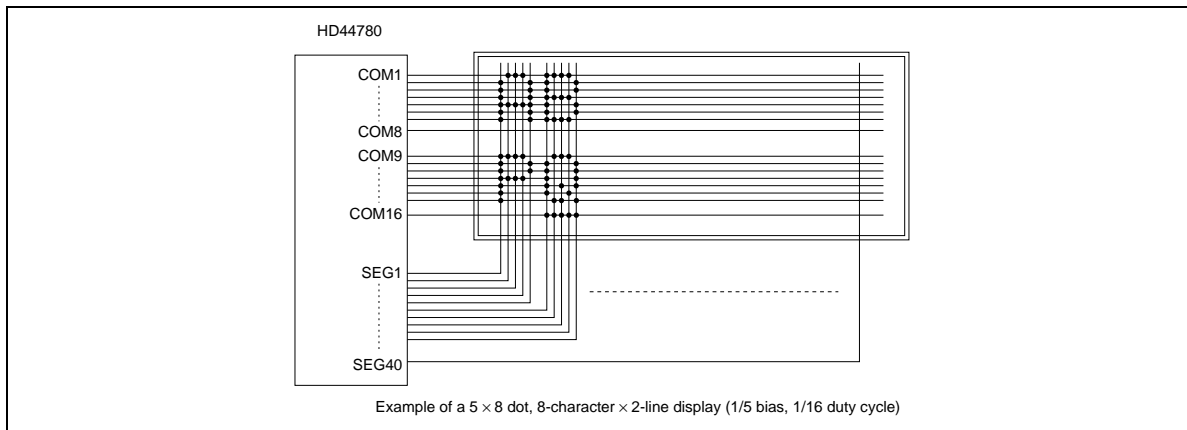


**Figure 20 Liquid Crystal Display and HD44780 Connections**

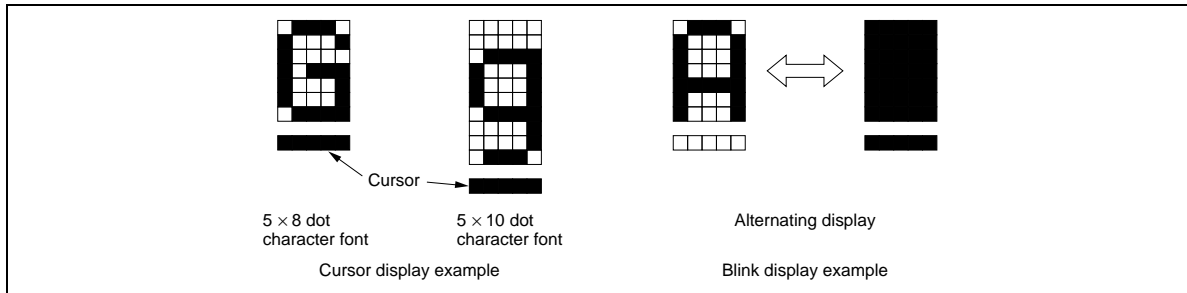
## HD44780U

Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in Figure 20 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (Figure 21).

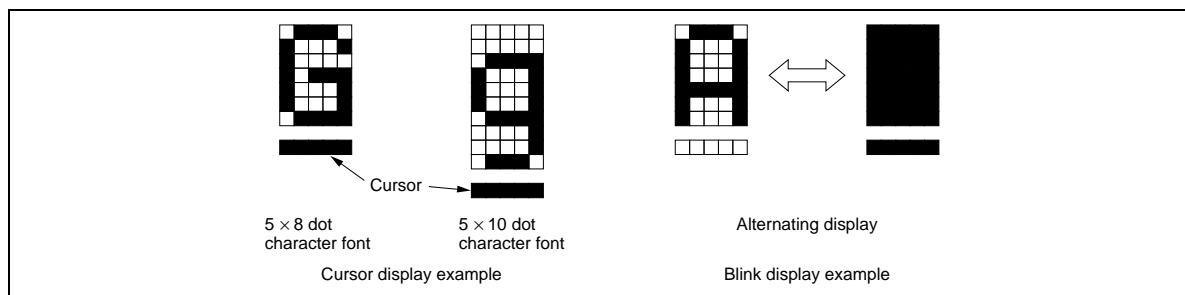


**Figure 20 Liquid Crystal Display and HD44780 Connections (cont)**



**Figure 21 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line**

**Connection of Changed Matrix Layout:** In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (Figure 22) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DDRAM) addresses for 4 characters  $\times$  2 lines and for 16 characters  $\times$  1 line are the same as in Figure 20.



**Figure 22 Changed Matrix Layout Displays**

## HD44780U

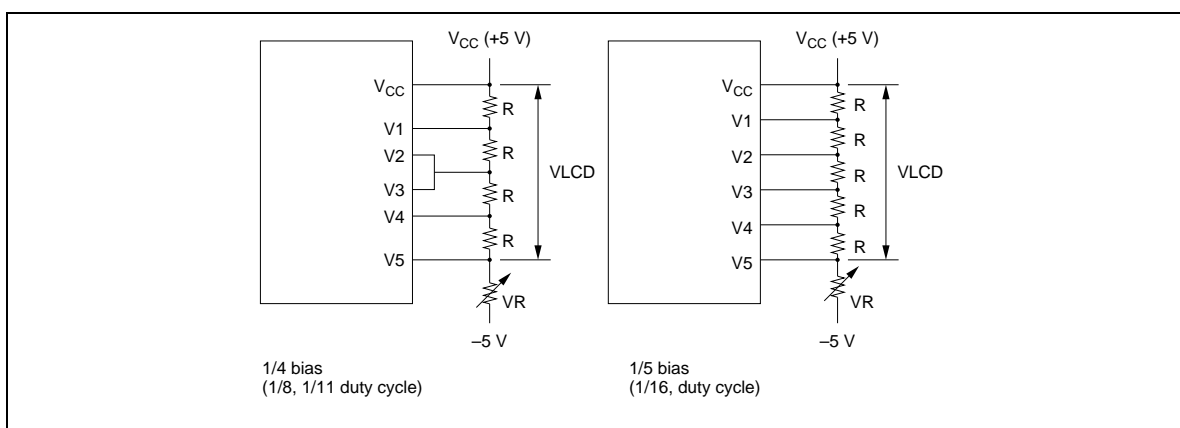
### Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V1 to V5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (Table 10).

VLCD is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V1 to V5 (Figure 23).

**Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive**

Power Supply	Duty Factor	
	1/8, 1/11	1/16
	Bias	
	1/4	1/5
V1	$V_{cc} - 1/4 \text{ VLCD}$	$V_{cc} - 1/5 \text{ VLCD}$
V2	$V_{cc} - 1/2 \text{ VLCD}$	$V_{cc} - 2/5 \text{ VLCD}$
V3	$V_{cc} - 1/2 \text{ VLCD}$	$V_{cc} - 3/5 \text{ VLCD}$
V4	$V_{cc} - 3/4 \text{ VLCD}$	$V_{cc} - 4/5 \text{ VLCD}$
V5	$V_{cc} - \text{VLCD}$	$V_{cc} - \text{VLCD}$



**Figure 23 Drive Voltage Supply Example**

## Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of Figure 24 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 μs).

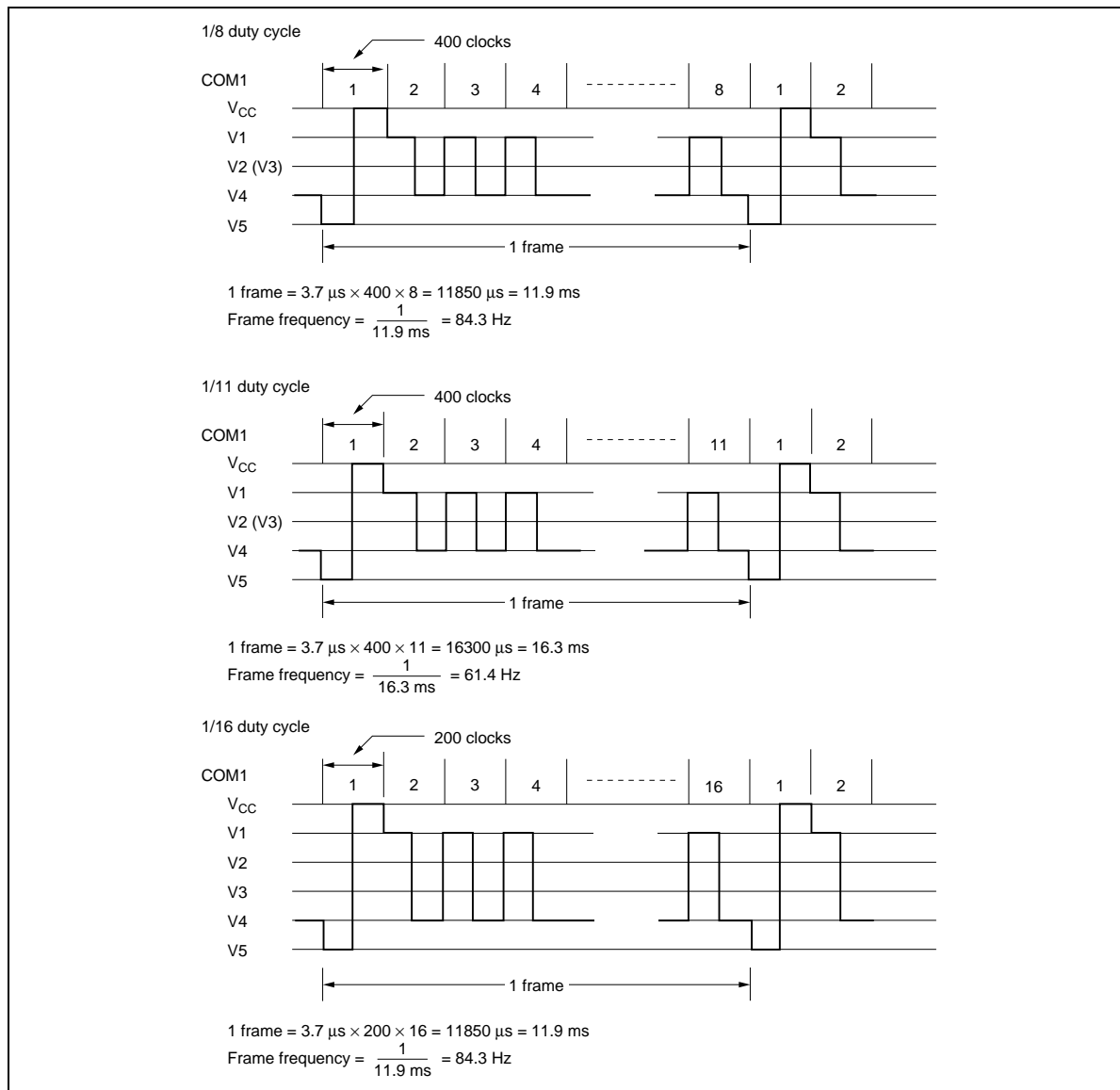


Figure 24 Frame Frequency

### **Instruction and Display Correspondence**

- 8-bit operation, 8-digit  $\times$  1-line display with internal reset

Refer to Table 11 for an example of an 8-digit  $\times$  1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

Since the display shift operation changes only the display position with DDRAM contents unchanged, the first display data entered into DDRAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit  $\times$  1-line display with internal reset

The program must set all functions prior to the 4-bit operation (Table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 12). Thus, DB4 to DB7 of the function set instruction is written twice.

- 8-bit operation, 8-digit  $\times$  2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be again set after the 8th character is completed. (See Table 13.) Note that the display shift operation is performed for the first and second lines. In the example of Table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

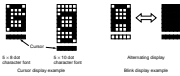


**Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset**


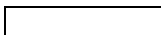
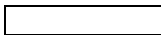

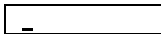

Step No.	Instruction	Display	Operation
1	Power supply on (the HD44780U is initialized by the internal reset circuit)	<input type="text"/>	Initialized. No display.
2	Function set 0 0 0 0 1 1 0 0 * *	<input type="text"/>	Sets to 8-bit operation and selects 1-line display and 5 × 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.)
3	Display on/off control 0 0 0 0 0 0 1 1 1 0	<input type="text"/>	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	<input type="text"/>	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	<input type="text" value="H_"/>	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 1	<input type="text" value="HI_"/>	Writes I.
7		<input type="text"/>	
8	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 1	<input type="text" value="HITACHI_"/>	Writes I.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	<input type="text" value="HITACHI_"/>	Sets mode to shift display at the time of write.
10	Write data to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	<input type="text" value="ITACHI _"/>	Writes a space.

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**Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)**

Step	Instruction										Display	Operation
No.	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
11	Write data to CGRAM/DDRAM											Writes M.
	1	0	0	1	0	0	1	1	0	1		
12						.					.	
						.					.	
						.					.	
						.					.	
						.					.	
13	Write data to CGRAM/DDRAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
14	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Write data to CGRAM/DDRAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
17	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
18	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
19	Write data to CGRAM/DDRAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
20						.					.	
						.					.	
						.					.	
						.					.	
						.					.	
21	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

**Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset**

Step		Instruction					Display	Operation
No.	RS	R/W	DB7	DB6	DB5	DB4		
1	Power supply on (the HD44780U is initialized by the internal reset circuit)							Initialized. No display.
2	Function set 0 0 0 0 1 0							Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function set 0 0 0 0 1 0 0 0 0 0 * *							Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.)
4	Display on/off control 0 0 0 0 0 0 0 0 1 1 1 0							Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0							Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
6	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 1 0 0 0							Writes H. The cursor is incremented by one and shifts to the right.

Note: The control is the same as for 8-bit operation beyond step #6.

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**Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset**

Step	Instruction										Display	Operation
No.	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	Power supply on (the HD44780U is initialized by the internal reset circuit)										<div></div> <div></div>	Initialized. No display.
2	Function set 0 0 0 0 1 1 1 0 * *										<div></div> <div></div>	Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font.
3	Display on/off control 0 0 0 0 0 0 1 1 1 0										<div>—</div> <div></div>	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0										<div>—</div> <div></div>	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0										<div>H—</div> <div></div>	Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.
6												
7	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 1										<div>HITACHI—</div> <div></div>	Writes I.
8	Set DDRAM address 0 0 1 1 0 0 0 0 0 0										<div>HITACHI</div> <div>—</div>	Sets DDRAM address so that the cursor is positioned at the head of the second line.

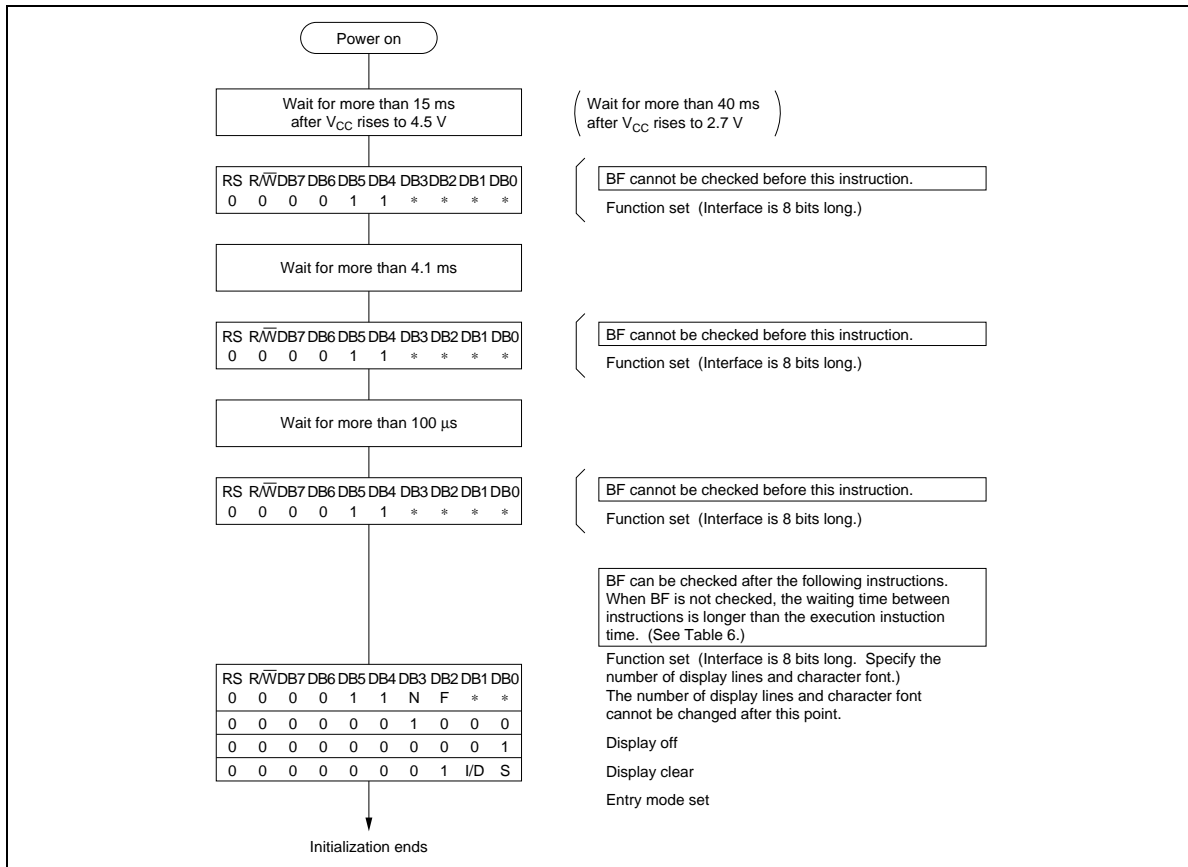
**Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)**

Step	Instruction											Display	Operation
No.	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
9	Write data to CGRAM/DDRAM											<div>HITACHI</div> <div>M_</div>	Writes M.
	1	0	0	1	0	0	1	1	0	1			
10													
11	Write data to CGRAM/DDRAM											<div>HITACHI</div> <div>MICROCO_</div>	Writes O.
	1	0	0	1	0	0	1	1	1	1			
12	Entry mode set											<div>HITACHI</div> <div>MICROCO_</div>	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1			
13	Write data to CGRAM/DDRAM											<div>ITACHI</div> <div>ICROCOM_</div>	Writes M. Display is shifted to the left. The first and second lines both shift at the same time.
	1	0	0	1	0	0	1	1	0	1			
14													
15	Return home											<div>HITACHI</div> <div>MICROCOM</div>	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0			

## Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to Figures 25 and 26 for the procedures on 8-bit and 4-bit initializations, respectively.



**Figure 25 8-Bit Interface**

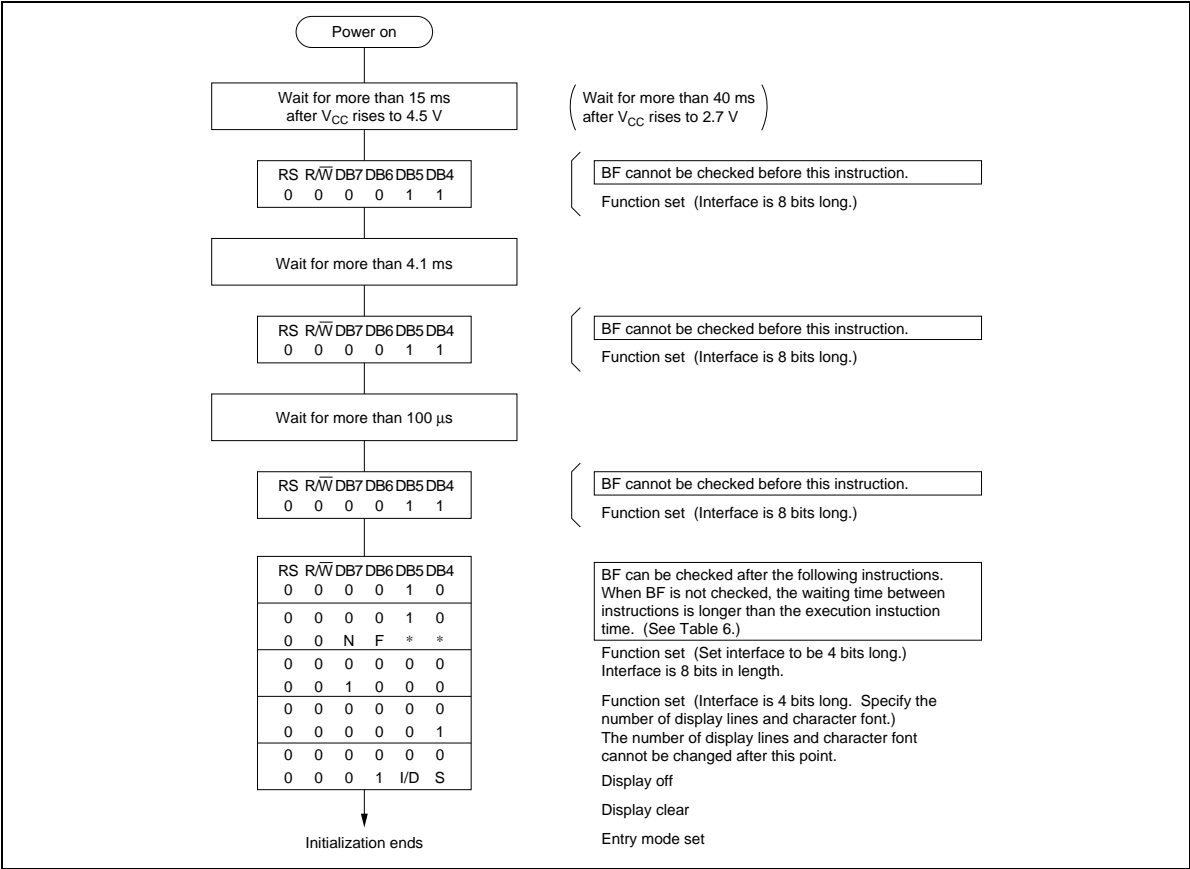


Figure 26 4-Bit Interface

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## HD44780U

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### Absolute Maximum Ratings\*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	$V_{CC}-GND$	-0.3 to +7.0	V	1
Power supply voltage (2)	$V_{CC}-V_5$	-0.3 to +13.0	V	1, 2
Input voltage	$V_t$	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature	$T_{opr}$	-20 to +75	°C	
Storage temperature	$T_{stg}$	-55 to +125	°C	4

Note: \* If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.



**DC Characteristics ( $V_{CC} = 2.7$  to  $4.5$  V,  $T_a = -20$  to  $+75^\circ\text{C}^{*3}$ )**

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	$0.7V_{CC}$	—	$V_{CC}$	V		6
Input low voltage (1) (except OSC1)	VIL1	-0.3	—	0.55	V		6
Input high voltage (2) (OSC1)	VIH2	$0.7V_{CC}$	—	$V_{CC}$	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (DB0–DB7)	VOH1	$0.75V_{CC}$	—	—	V	$-I_{OH} = 0.1$ mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	$0.2V_{CC}$	V	$I_{OL} = 0.1$ mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	$0.8V_{CC}$	—	—	V	$-I_{OH} = 0.04$ mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	$0.2V_{CC}$	V	$I_{OL} = 0.04$ mA	8
Driver on resistance (COM)	$R_{COM}$	—	2	20	k $\Omega$	$\pm I_d = 0.05$ mA, VLCD = 4 V	13
Driver on resistance (SEG)	$R_{SEG}$	—	2	30	k $\Omega$	$\pm I_d = 0.05$ mA, VLCD = 4 V	13
Input leakage current	$I_{LI}$	-1	—	1	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$	9
Pull-up MOS current (DB0–DB7, RS, R/W)	$-I_p$	10	50	120	$\mu\text{A}$	$V_{CC} = 3$ V	
Power supply current	$I_{CC}$	—	0.15	0.30	mA	$R_f$ oscillation, external clock $V_{CC} = 3$ V, $f_{osc} = 270$ kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	$V_{CC} - V_5$ , 1/5 bias	16
	VLCD2	3.0	—	11.0	V	$V_{CC} - V_5$ , 1/4 bias	16

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

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### AC Characteristics ( $V_{CC} = 2.7$ to $4.5$ V, $T_a = -20$ to $+75^\circ\text{C}^{*3}$ )

#### Clock Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Note*
External clock operation	External clock frequency	$f_{cp}$	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	$t_{rcp}$	—	—	0.2	$\mu\text{s}$		
	External clock fall time	$t_{fcp}$	—	—	0.2	$\mu\text{s}$		
$R_i$ oscillation	Clock oscillation frequency	$f_{osc}$	190	270	350	kHz	$R_i = 75\text{ k}\Omega$ , $V_{CC} = 3\text{ V}$	12

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

#### Bus Timing Characteristics

##### Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	$t_{cycE}$	1000	—	—	ns	Figure 27
Enable pulse width (high level)	$PW_{EH}$	450	—	—		
Enable rise/fall time	$t_{Er}$ , $t_{Ef}$	—	—	25		
Address set-up time (RS, $\overline{R/\overline{W}}$ to E)	$t_{AS}$	60	—	—		
Address hold time	$t_{AH}$	20	—	—		
Data set-up time	$t_{DSW}$	195	—	—		
Data hold time	$t_H$	10	—	—		

##### Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	$t_{cycE}$	1000	—	—	ns	Figure 28
Enable pulse width (high level)	$PW_{EH}$	450	—	—		
Enable rise/fall time	$t_{Er}$ , $t_{Ef}$	—	—	25		
Address set-up time (RS, $\overline{R/\overline{W}}$ to E)	$t_{AS}$	60	—	—		
Address hold time	$t_{AH}$	20	—	—		
Data delay time	$t_{DDR}$	—	—	360		
Data hold time	$t_{DHR}$	5	—	—		

**Interface Timing Characteristics with External Driver**

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	$t_{CWH}$	800	—	—	ns	Figure 29
	Low level	$t_{CWL}$	800	—	—		
Clock set-up time		$t_{CSU}$	500	—	—		
Data set-up time		$t_{SU}$	300	—	—		
Data hold time		$t_{DH}$	300	—	—		
M delay time		$t_{DM}$	−1000	—	1000		
Clock rise/fall time		$t_{ct}$	—	—	200		

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**Power Supply Conditions Using Internal Reset Circuit**

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time		$t_{rCC}$	0.1	—	10	ms	Figure 30
Power supply off time		$t_{OFF}$	1	—	—		

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## HD44780U

### DC Characteristics ( $V_{CC} = 4.5$ to $5.5$ V, $T_a = -20$ to $+75^\circ\text{C}^{*3}$ )

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC1)	VIH1	2.2	—	$V_{CC}$	V		6
Input low voltage (1) (except OSC1)	VIL1	-0.3	—	0.6	V		6
Input high voltage (2) (OSC1)	VIH2	$V_{CC}-1.0$	—	$V_{CC}$	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	1.0	V		15
Output high voltage (1) (DB0–DB7)	VOH1	2.4	—	—	V	$-I_{OH} = 0.205$ mA	7
Output low voltage (1) (DB0–DB7)	VOL1	—	—	0.4	V	$I_{OL} = 1.2$ mA	7
Output high voltage (2) (except DB0–DB7)	VOH2	$0.9 V_{CC}$	—	—	V	$-I_{OH} = 0.04$ mA	8
Output low voltage (2) (except DB0–DB7)	VOL2	—	—	$0.1 V_{CC}$	V	$I_{OL} = 0.04$ mA	8
Driver on resistance (COM)	RCOM	—	2	20	k $\Omega$	$\pm I_d = 0.05$ mA, VLCD = 4 V	13
Driver on resistance (SEG)	RSEG	—	2	30	k $\Omega$	$\pm I_d = 0.05$ mA, VLCD = 4 V	13
Input leakage current	$I_{LI}$	-1	—	1	$\mu\text{A}$	$V_{IN} = 0$ to $V_{CC}$	9
Pull-up MOS current (DB0–DB7, RS, R/W)	$-I_p$	50	125	250	$\mu\text{A}$	$V_{CC} = 5$ V	
Power supply current	$I_{CC}$	—	0.35	0.60	mA	$R_f$ oscillation, external clock $V_{CC} = 5$ V, $f_{OSC} = 270$ kHz	10, 14
LCD voltage	VLCD1	3.0	—	11.0	V	$V_{CC}-V_5$ , 1/5 bias	16
	VLCD2	3.0	—	11.0	V	$V_{CC}-V_5$ , 1/4 bias	16

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**AC Characteristics ( $V_{CC} = 4.5$  to  $5.5$  V,  $T_a = -20$  to  $+75^\circ\text{C}^{*3}$ )**
**Clock Characteristics**

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	$f_{cp}$	125	250	350	kHz		11
	External clock duty	Duty	45	50	55	%		11
	External clock rise time	$t_{rcp}$	—	—	0.2	$\mu\text{s}$		11
	External clock fall time	$t_{fcp}$	—	—	0.2	$\mu\text{s}$		11
$R_f$ oscillation	Clock oscillation frequency	$f_{osc}$	190	270	350	kHz	$R_f = 91\text{ k}\Omega$ $V_{CC} = 5.0\text{ V}$	12

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**Bus Timing Characteristics**
**Write Operation**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	$t_{cycE}$	500	—	—	ns	Figure 27
Enable pulse width (high level)	$PW_{EH}$	230	—	—		
Enable rise/fall time	$t_{Er}, t_{Ef}$	—	—	20		
Address set-up time (RS, $\overline{R/\overline{W}}$ to E)	$t_{AS}$	40	—	—		
Address hold time	$t_{AH}$	10	—	—		
Data set-up time	$t_{DSW}$	80	—	—		
Data hold time	$t_H$	10	—	—		

**Read Operation**

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	$t_{cycE}$	500	—	—	ns	Figure 28
Enable pulse width (high level)	$PW_{EH}$	230	—	—		
Enable rise/fall time	$t_{Er}, t_{Ef}$	—	—	20		
Address set-up time (RS, $\overline{R/\overline{W}}$ to E)	$t_{AS}$	40	—	—		
Address hold time	$t_{AH}$	10	—	—		
Data delay time	$t_{DDR}$	—	—	160		
Data hold time	$t_{DHR}$	5	—	—		

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## HD44780U

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### Interface Timing Characteristics with External Driver

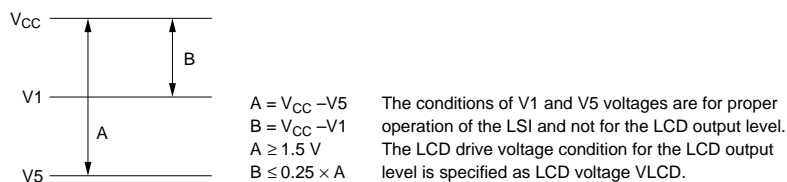
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	$t_{CWH}$	800	—	—	ns	Figure 29
	Low level	$t_{CWL}$	800	—	—		
Clock set-up time		$t_{CSU}$	500	—	—		
Data set-up time		$t_{SU}$	300	—	—		
Data hold time		$t_{DH}$	300	—	—		
M delay time		$t_{DM}$	–1000	—	1000		
Clock rise/fall time		$t_{ct}$	—	—	100		

### Power Supply Conditions Using Internal Reset Circuit

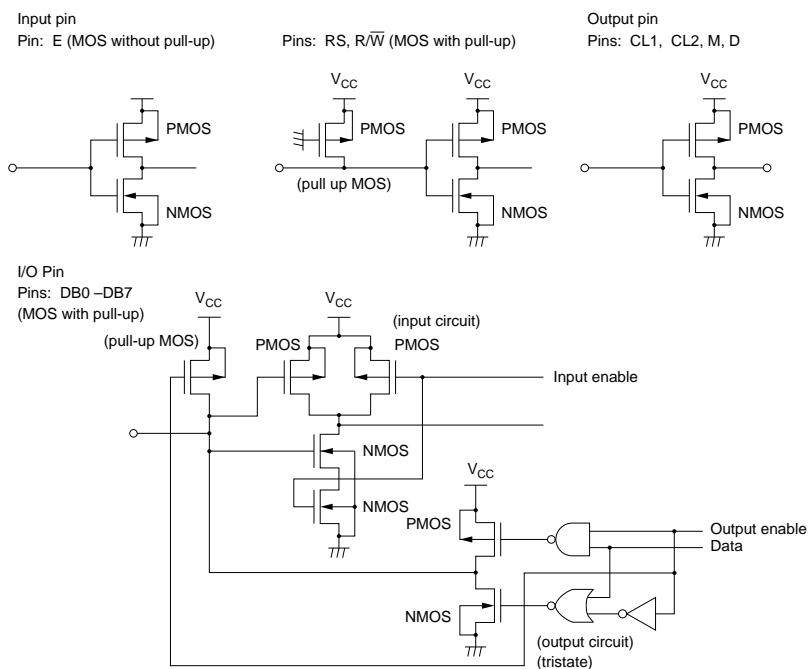
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time		$t_{ICC}$	0.1	—	10	ms	Figure 30
Power supply off time		$t_{OFF}$	1	—	—		

## Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V.

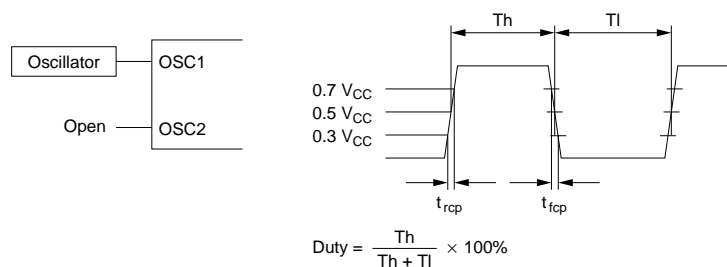


2.  $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$  must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

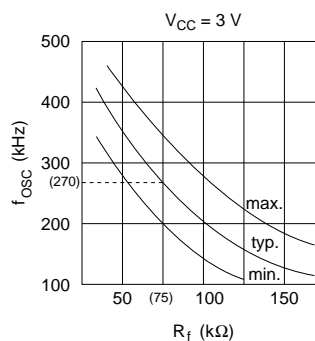
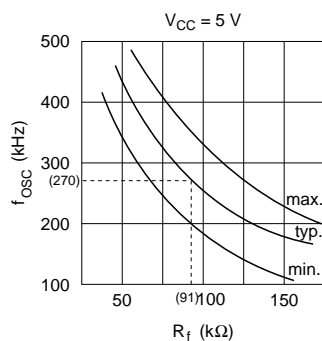
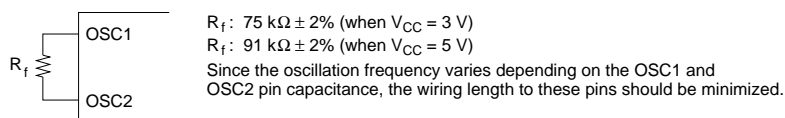


## HD44780U

6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



12. Applies only to the internal oscillator operation using oscillation resistor  $R_f$ .

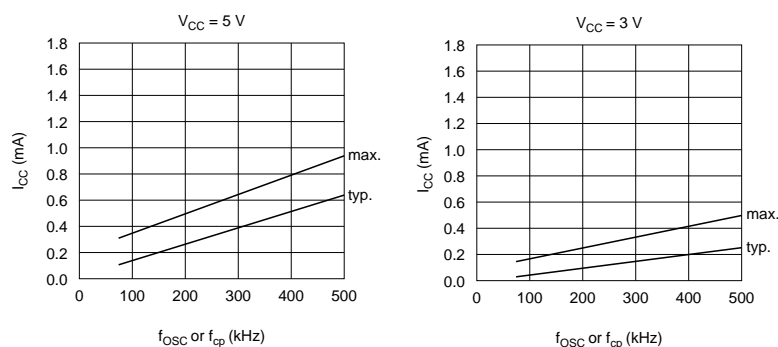




13. RCOM is the resistance between the power supply pins ( $V_{CC}$ , V1, V4, V5) and each common signal pin (COM1 to COM16).

RSEG is the resistance between the power supply pins ( $V_{CC}$ , V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

14. The following graphs show the relationship between operation frequency and current consumption.

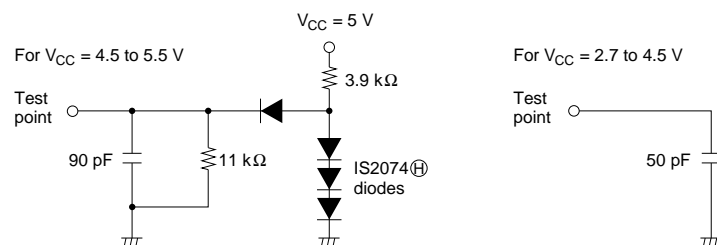


15. Applies to the OSC1 pin.

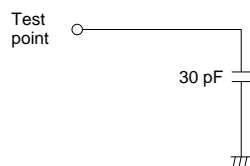
16. Each COM and SEG output voltage is within  $\pm 0.15V$  of the LCD voltage ( $V_{CC}$ , V1, V2, V3, V4, V5) when there is no load.

## Load Circuits

### Data Bus DB0 to DB7



### External Driver Control Signals: CL1, CL2, D, M



Timing Characteristics

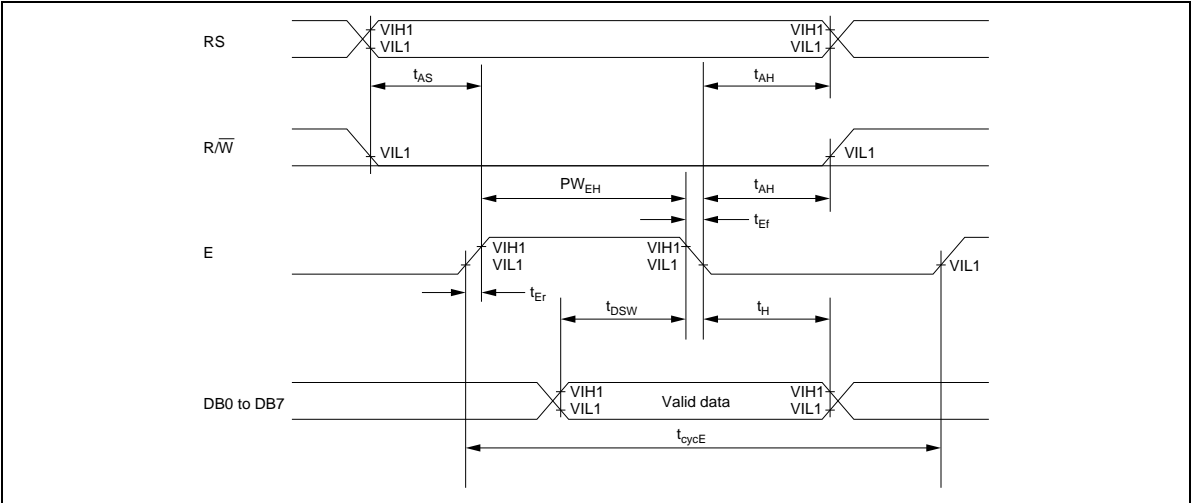


Figure 27 Write Operation

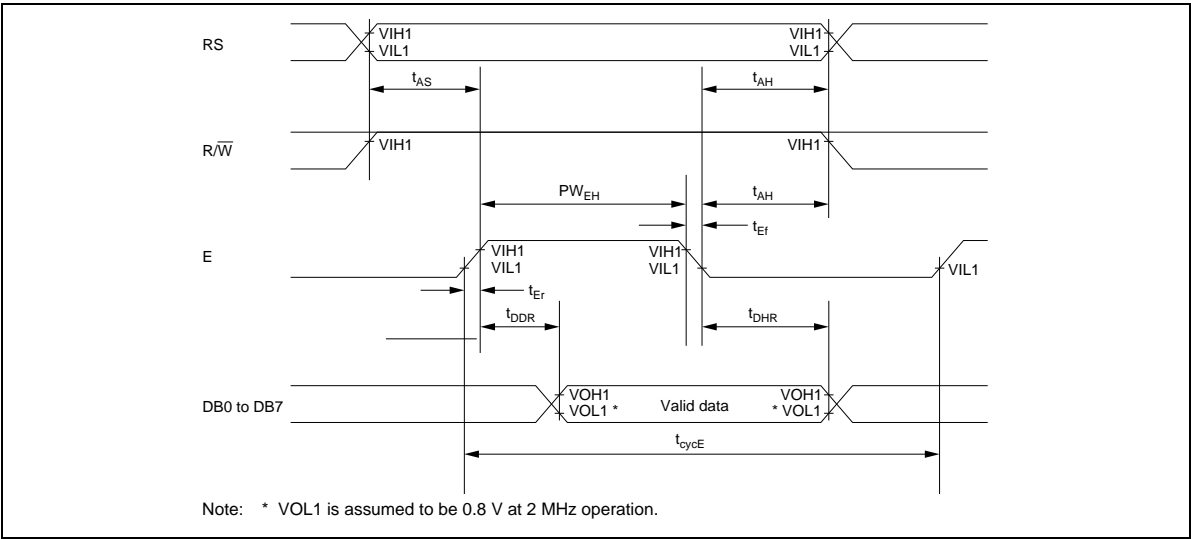
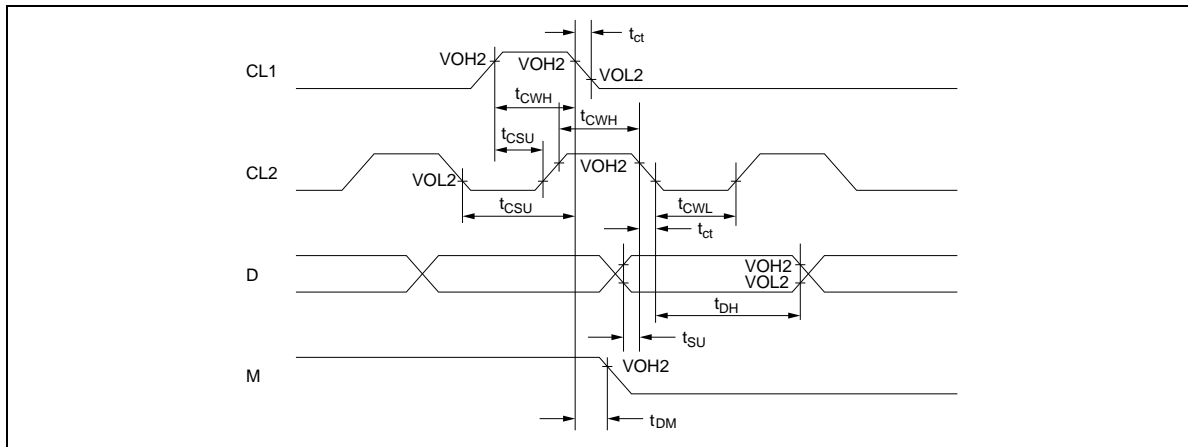
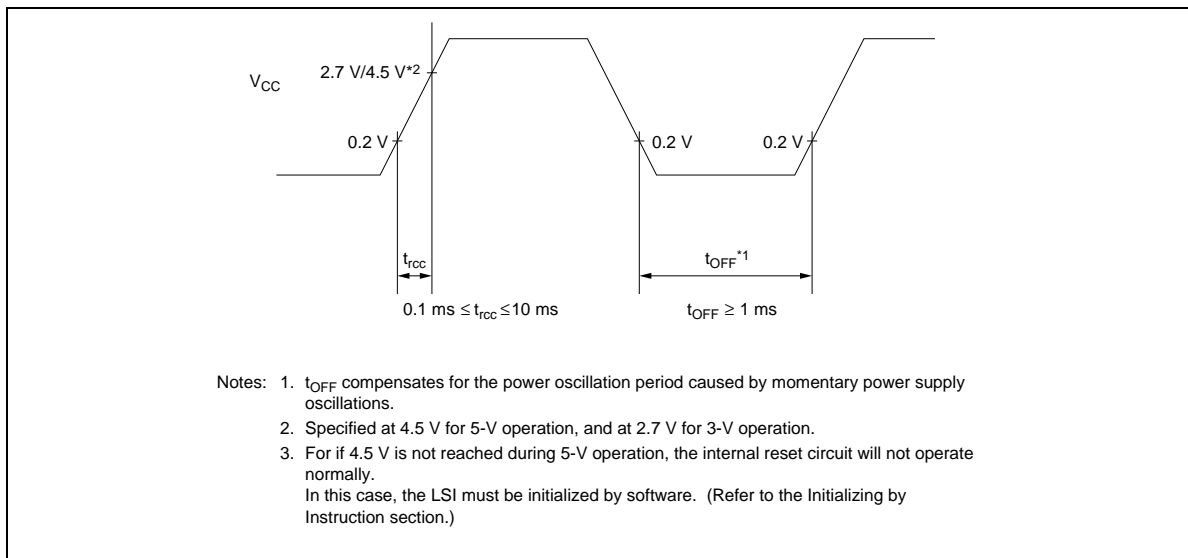


Figure 28 Read Operation



**Figure 29 Interface Timing with External Driver**



**Figure 30 Internal Power Supply Reset**